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L2	5	"circuit design" and component and third and "rule object" and run-time and @ad<"20030820"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/11/06 11:29
L3	6	circuit.clm. and design.clm. and rule.clm. and component.clm. and object.clm. and @ad<"20030820"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/11/06 11:50
L4	124	rule and application and "circuit design" and object and runtime and @ad<"20030820" and @pd>"20030330"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/11/06 12:05
L5	14	706/47 and 706/46 and 706/14 and @ad<"20030820" and @pd>"20030330"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/11/06 12:09
L6	2103	716/5 and @ad<"20030820"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/11/06 12:09
L7	319	6 and "circuit design" and rule and object	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/11/06 12:10
L8	32	7 and component and trigger	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/11/06 12:10



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Test Conference, 1990. Proceedings., International  
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Digital Object Identifier 10.1109/TEST.1990.114130  
AbstractPlus | Full Text: [PDF\(824 KB\)](#) **IEEE CNF**  
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**object-oriented modeling**  
Khawaja, A.A.;  
Computer Software and Applications Conference, 1997. C  
Proceedings., The Twenty-First Annual International  
13-15 Aug. 1997 Page(s):104 - 108  
Digital Object Identifier 10.1109/CMPASAC.1997.624771  
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**electronic circuit design**  
Cumbi, M.J.N.; Shepherd, D.W.; Hulley, L.N.;  
Power Electronics, IEEE Transactions on  
Volume 11, Issue 3, May 1996 Page(s):393 - 404  
Digital Object Identifier 10.1109/63.491632  
AbstractPlus | [References](#) | Full Text: [PDF\(920 KB\)](#) **IEEE**  
[Rights and Permissions](#)
- ☐ 4. **Developing a distributed architecture for design rule c**  
Pais, A.P.V.; Anido, M.L.; Oliveira, C.E.T.;  
Circuits and Systems, 2001. MWSCAS 2001. Proceedings  
2001 Midwest Symposium on  
Volume 2, 14-17 Aug. 2001 Page(s):678 - 681 vol.2  
Digital Object Identifier 10.1109/MWSCAS.2001.986279  
AbstractPlus | Full Text: [PDF\(217 KB\)](#) **IEEE CNF**

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- ☐ **5. An object-oriented concept for intelligent library funct**  
Oberg, J.; Kumar, A.; Jantsch, A.;  
VLSI Design, 1998. Proceedings., 1998 Eleventh Internati  
4-7 Jan. 1998 Page(s):355 - 358  
Digital Object Identifier 10.1109/ICVD.1998.646632  
[AbstractPlus](#) | [Full Text: PDF\(412 KB\)](#) **IEEE CNF**  
[Rights and Permissions](#)
  
- ☐ **6. Design and analysis of electric circuits using Java**  
Lazareck, L.; Peters, J.F.;  
Electrical and Computer Engineering, 2001. Canadian Cor  
Volume 2, 13-16 May 2001 Page(s):851 - 856 vol.2  
Digital Object Identifier 10.1109/CCECE.2001.933552  
[AbstractPlus](#) | [Full Text: PDF\(516 KB\)](#) **IEEE CNF**  
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- ☐ **7. Metaprogramming in digital simulation**  
Eicher, J.W.; Brown, F.M.;  
Aerospace and Electronics Conference, 1995. NAECON 1  
the IEEE 1995 National  
Volume 2, 22-26 May 1995 Page(s):659 - 663 vol.2  
Digital Object Identifier 10.1109/NAECON.1995.522007  
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- ☐ **8. A new approach to perform circuit verification using O**  
Nunes, R.B.; Anido, M.L.; Olivera, C.E.T.;  
EUROMICRO 94. System Architecture and Integration. Pr  
20th EUROMICRO Conference.  
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Digital Object Identifier 10.1109/EURMIC.1994.390415  
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- ☐ **9. The schema-based approach to workflow managemen**  
Brockman, J.B.; Director, S.W.;  
Computer-Aided Design of Integrated Circuits and System  
on  
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Digital Object Identifier 10.1109/43.466341  
[AbstractPlus](#) | [Full Text: PDF\(1116 KB\)](#) **IEEE JNL**  
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Li-Rong Zheng; Bingxin Li; Tenhunen, H.;  
ASIC/SOC Conference, 1999. Proceedings. Twelfth Annu  
15-18 Sept. 1999 Page(s):251 - 256  
Digital Object Identifier 10.1109/ASIC.1999.806514  
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